REMARKS

This paper is being filed as a response to the Office Action of October 28, 2008. Reconsideration is respectfully requested in view of these remarks.

First Rejection under 35 USC § 103(a)

Claims 1, 2, 4, 5, 8-11, and 14-16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Amagai et al. (US Patent No. 7,130,312), in view of Soejima et al. (U.S. Patent No. 6,654,823). This rejection is respectfully traversed. Applicants respectfully request reconsideration of these rejections in light of the arguments contained herein.

Claim 1 teaches defining a pipeline of processors in communication with a distributed network and a central processing unit (CPU) of a host system (emphasis added). The Office has asserted that Amagai teaches this feature in "Fig. 7, where three processes are performed" (page 2, parg. 6 - emphasis added). Applicants respectfully disagree.

As asserted by the Examiner, Fig. 7, merely presents three processes. A process is something intangible that exists within the logic of a computer system. On the other hand, a processor is something tangible, part of the structure of a system. Thus, a process does not anticipate a processor. Further, the rejection by the Office seems to imply that three processes performed simultaneously implies the use of three different processors. However, the person skilled in the art will readily appreciate that one processor can process several processes simultaneously, thus implying that three processes requires multiple processors would be erroneous. For all these reasons, Amagai does not suggest a pipeline of processors as claimed by Applicants. It should be noted that the Offices has asserted that process A, B, and C teach the plurality of processors, which is inconsistent with other rejections from the Office, as discussed below.

Further, claim 1 defines repeating the operations of processing **the** data packet and transmitting the processed data packet for successive stages (emphasis added). The Office has asserted that Amagai teaches this feature in "Fig. 7, where X, Y, Z, are layered (stages) processing portions repeating operations for different packets" (page 2, last paragraph - emphasis added). Applicants respectfully disagree.

Assuming *arguendo* that Amagai teaches repeating operations for different packets, as asserted by the Office, Applicants claimed repeating operations of processing the data packet, that is, the operations are performed on the same packet. The Office has not shown how Amagai teaches this feature because the Office has only arguably shown how to repeat operations for different packets, thus the Office's rejection is improper. Further, if should be noted that if processes A, B, and C correspond to different processors, as previously discussed, the operations on a packet are all performed by the same "processor/process." However, Applicants define that each stage of processing for a data packet corresponds to a different processor (see claim 1), i.e., each stage of processing on a data packet is done by a different processor. Accordingly, Amagai processes the data packets differently than the claimed embodiments of the present Appliction. For all these reasons, Amagai does not teach the claimed features.

In addition, claim 1 defines processing the data packet to remove a header associated with the first stage, and repeating the operations of processing the data packet and transmitting the processed data packet for successive stages associated with corresponding processors until a header associated with a final stage has been removed from the data packet (emphasis added). The Office has asserted that these features are taught by Soejima in "column 17, lines 1-10, describing the decapsulation process of the headers i.e. PPP header,

UDP header, IP header, etc using the pipelined processors i.e. processing units [68#1j] where j=1 to m" (page 3, parg. 4 - emphasis added). Applicants respectfully disagree.

With respect to the rejection of claim 1, the Office has also asserted that Soejima teaches "a pipeline of processors, i.e. [2], [6], [10], and [12]" (page 3, parg. 4 - emphasis added) in Fig. 1. If the Office asserts that Soejima teaches a pipeline of processors [2], [6], [10], and [12], then the Office should refer to those processors when referring to the processors in the rejection of claim 1. However, the Office then changes the plurality of processors to become processing units [68#1j]. The Office lacks consistency in the rejection of claim 1, and the rejection is improper.

The Examiner is also reminded that the claimed invention as a whole must be considered. In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983).

"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). The Office has failed to analyze Applicant's claims as a whole, instead breaking down rejections into pieces that lack logic and do not show how the prior art teaches the featured claims.

Moreover, the processing units [68#1j] taught by Soejima do not suggest the features claimed. The Office has used the excerpt below in the rejection of Applicants' claims:

> "If they match each other, on the other hand, the packet is supplied to the packet-data post-processors 68#1j where j=1 to m for deleting the PPP header, the UDP header and the IP header. Then, routing information is detected before the packet is passed on to the switch

> fabric 50. The switch fabric 50 carries out routing on the packet in accordance with the routing information and then supplies the packet to a transmission IF unit 52#i for the route, for example, the transmission IF unit 52#1. The transmission interface unit 54#1 then outputs the packet to the private network 38" (col. 17, lines 1-10 - emphasis added).

Soejima teaches post-processors 68#1j for deleting the PPP header, the UDP header and the IP header. However, Soejima does not teach that each stage (associated with the corresponding processor) removes a header. Thus, the Office's rejection is improper.

Independent claims 8 and 14 are believed to be patentable for at least the same reasons as with respect to claim 1. In view of the foregoing, the Office is requested to withdraw the rejection of claims 1, 8, and 14 under §103.

Additional Rejections under 35 USC § 103(a)

Claims 3, 12, and 17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Amagai in view of Soejima, and further in view of Wong et al. (US Patent No. 9,963,563).

Claims 6, 7, 13, 18, and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Amagai in view of Soejima, and further in view of **Chandra** et al. (US Patent No.7,185,153).

Claim 19 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Amagai in view of Soejima and **Chandra**, and further in view of Kejriwal et al. (US Patent No. 6,704,794).

These rejections are respectfully traversed.

The Office has used Chandra as a prior art reference in several rejections, but Chandra's Patent was filed on December 18, 2003, which is posterior to Applicants' priority date of December 12, 2002. Therefore, **Chandra is not a valid reference** for rejecting Applicants' claims, and the Office's rejections are improper. Additionally, the Office has not listed the Chandra and the Amagai references under the Notice of References Cited. Applicants respectfully request that the Office accurately reflects the prior art documents used in the rejections in the Notice of References Cited section.

Further, Applicants respectfully request that the rejections of dependent claims 3, 6, 7, 12, 13, and 17- 20 be withdrawn, as the added references do not cure the deficiencies in the rejections of the independent claims. The dependent claims are submitted to be patentable for at least the same reasons the independent claims are believed to be patentable. The Applicants therefore respectfully request reconsideration and allowance of the pending claims. A Notice of Allowance is respectfully requested.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6920. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP236).

Respectfully submitted,
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